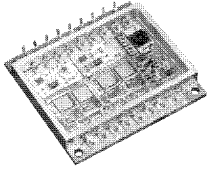


## SMART POWER H-BRIDGE MOTOR DRIVES



### FEATURES

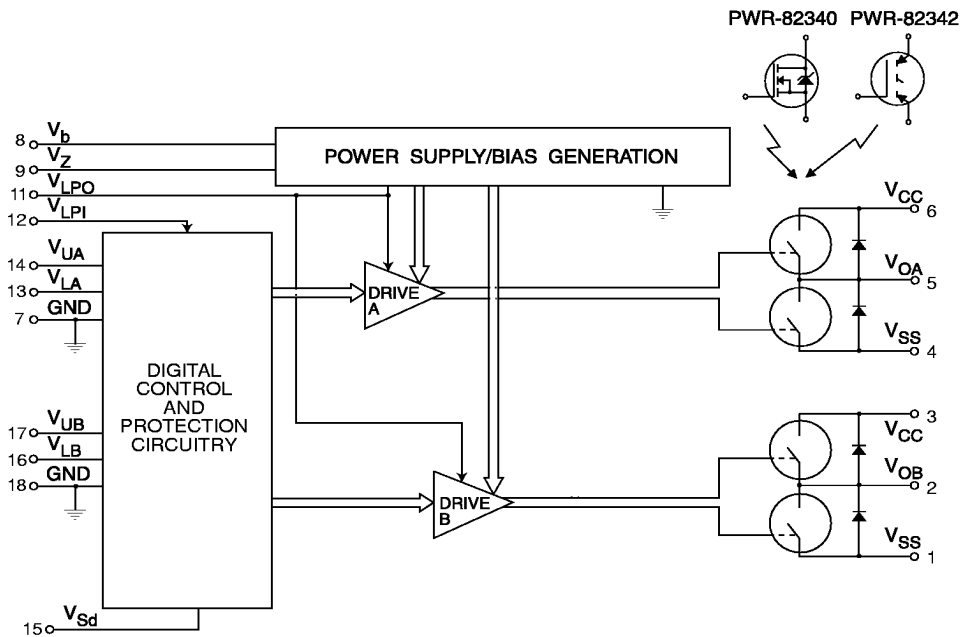
- **Small Size (2.25" x 2.1" x 0.39")**
- **200 V and 500 V Capability**
- **30 A Current Capability**
- **High-Efficiency MOSFET or IGBT Drive Stage**
- **Direct Drive from PWM**
- **Drives Brushless DC or Brush Motors**
- **Four Quadrant Operation**
- **0.85 °C/W  $\theta_{j-c}$  Max**
- **Military Processing Available**

### DESCRIPTION

The PWR-82340 and PWR-82342 are 30 A H-bridge motor drive hybrids. The PWR-82340 has a 200 V rating and uses MOSFETs in the output stage while the PWR-82342 has a 500 V rating and an IGBT output stage. Both types have individual fast recovery diodes internally connected across the output drive transistors to clamp inductive flyback. This new series of Smart Power Motor Drives has CMOS Schmitt Trigger inputs for high noise immunity. High- and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn-on of in-line transistors, thus eliminating a shoot-thru condition. The internal logic controls the high- and low-side gate drives for each phase and can operate from +5 to +15 V logic levels. The internal power supply provides a constant voltage source to the floating high side gate drives. This provides constant output performance for switching frequencies from DC to 50 kHz.

### APPLICATIONS

Packaged in small cases, these hybrids are an excellent choice for high performance, high reliability motor drives for military and aerospace servo-amps and speed controls. Among the many applications are robotics; electro-mechanical valve assemblies; actuator systems for flight control surfaces on military and commercial aircraft; antenna and radar positioning; fan and blower motors for environmental conditioning; thrust and vector position control of mini subs, drones, and RPV's; compressor motors for cryogenic coolers; and high-power inverters. The PWR-82340/342 hybrids are ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications where fin actuator systems control missile direction. The PWR-82340 and PWR-82342 operate over the -55°C to +125°C temperature range and are available with military processing.



**FIGURE 1. PWR-82340/342 BLOCK DIAGRAM**

**TABLE 1. PWR-82340 AND PWR-82342 ABSOLUTE MAXIMUM RATINGS**  
 $T_C = +25^\circ\text{C}$  unless otherwise specified)

PARAMETER	SYMBOL	PWR-82340 VALUE	PWR-82342 VALUE	UNITS
SUPPLY VOLTAGE	$V_{CC}$	200	500	V
BIAS VOLTAGE	$V_b$	50	50	V
LOGIC POWER-IN VOLTAGE	$V_{LPI}$	18	18	V
INPUT LOGIC VOLTAGE	$V_U, V_L, V_{Sd}$	$V_{LPI} + 0.5$	$V_{LPI} + 0.5$	V
OUTPUT CURRENT CONTINUOUS	$I_o$	30	30	A
PULSED	$I_{op}$	50	50	A
OPERATING FREQUENCY	$f_o$	50	25	KHz
CASE OPERATING TEMPERATURE	$T_C$	-55 to +125	-55 to +125	$^\circ\text{C}$
CASE STORAGE TEMPERATURE	$T_{CS}$	-55 to +150	-55 to +150	$^\circ\text{C}$

**TABLE 2. PWR-82340 AND PWR-82342 SPECIFICATIONS**  
 $T_C = +25^\circ\text{C}$  unless otherwise specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	PWR-82340			PWR-82342			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
<b>OUTPUT</b>										
Output Current Continuous (see FIGURES 19 and 15)	$I_o$	see note 1			30			30	A	
Supply Voltage	$V_{CC}$		140		200	270		500	V	
Output On Resistance (each FET)(see FIGURE 14A)	$R_{on}$	$I_o = 30\text{ A}$			0.1				ohm	
Output Voltage Drop (each IGBT)(see FIGURES 14B)	$V_{CE(SAT)}$	$I_o = 30\text{ A}$						3.8	V	
Instant Forward Voltage (flyback diode)(see FIGURE 13)	$V_F$	$I_o = 30\text{ A}$ (see note 2)			1.15			1.70	V	
Reverse Recovery Time (flyback diode)	$t_{rr}$	$I_f = 1\text{ A}, I_r = 1\text{ A}$			50			50	nsec	
Reverse Leakage Current at $T_C = +25^\circ\text{C}$	$I_r$	see note 3			10			10	$\mu\text{A}$	
Reverse Leakage Current at $T_C = +125^\circ\text{C}$	$I_r$	see note 3			1			1	mA	
<b>BIAS SUPPLY</b>										
Input Bias Voltage ( $T_C = -55$ to $+125^\circ\text{C}$ )	$V_b$	$V = 28\text{ V}$	14		50	15		50	V	
Quiescent Bias Current (see note 4)(see FIGURE 16)	$I_{bq}$	$V_b = 28\text{ V}$ (see note 5)		27			27		mA	
Bias Current ( $T_C = -55$ to $+125^\circ\text{C}$ ) (see FIGURES 17 and 18)	$I_b$		30		40	24		35	mA	
Inrush Current ( $T_C = -55$ to $+125^\circ\text{C}$ )	$I_{ir}$	$V_b = 28\text{ V}$			1.4			1.4	A	
Logic Power Input Current	$I_{LPI}$	see note 6			2			2	mA	
<b>INPUT SIGNALS (see FIGURE 7)</b>										
Positive Trigger Threshold Voltage	$V_P$	<b>Pin Connections</b> Pin 11 and 12 connected	6.8		10	6.8		10	V	
Negative Trigger Threshold Voltage	$V_N$	Pin 11 and 12 connected	4.0		7	4.0		7	V	
Positive Trigger Threshold Voltage	$V_P$	see note 6	2.2		3	2.2		3	V	
Negative Trigger Threshold Voltage	$V_N$	see note 6	0.9		2	0.9		2	V	
<b>SWITCHING CHARACTERISTICS (see FIGURE 2)</b>										
<b>Upper Drive:</b>										
Turn-on propagation delay	$t_d$ (on)	<b>Test 1 Conditions</b> Pin 11 and 12 connected +15 V logic $I_o = 30\text{ A}$ peak PWR-82340 $V_{CC} = 140\text{ V}$ PWR-82342 $V_{CC} = 270\text{ V}$			840			810	nsec	
Turn-off propagation delay	$t_d$ (off)		1020			860			nsec	
Shut down propagation delay	$t_{Sd}$		800			810			nsec	
Turn-on rise time	$t_r$		125			100			nsec	
Turn-off fall time	$t_f$		125			150			nsec	
<b>Lower Drive:</b>										
Turn-on propagation delay	$t_d$ (on)					850			800	nsec
Turn-off propagation delay	$t_d$ (off)					1000			870	nsec
Shut down propagation delay (see FIGURE 9)	$t_{Sd}$					800			770	nsec
Turn-on rise time	$t_r$					125			100	nsec
Turn-off fall time	$t_f$				125			150	nsec	
<b>SWITCHING CHARACTERISTICS (see FIGURE 2)</b>										
<b>Upper Drive:</b>										
Turn-on propagation delay	$t_d$ (on)	<b>Test 2 Conditions</b> see note 6 +5 V logic			1090			1050	nsec	
Turn-off propagation delay	$t_d$ (off)	$I_o = 30\text{ A}$ peak			1315			1150	nsec	
Shut down propagation delay	$t_{Sd}$	PWR-82340			1100			850	nsec	
Turn-on rise time	$t_r$	$V_{CC} = 140\text{ V}$			125			100	nsec	
Turn-off fall time	$t_f$	PWR-82342 $V_{CC} = 270\text{ V}$			125			150	nsec	

**TABLE 2. PWR-82340 AND PWR-82342 SPECIFICATIONS (CONTINUED)**  
( $T_C = 25^\circ\text{C}$  unless otherwise specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	PWR 82340			PWR 82342			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCHING CHARACTERISTICS (continued)</b>									
<b>LowerDrive:</b>									
Turn-on propagation delay	$t_{d(on)}$	see note 6			1125			1050	nsec
Turn-off propagation delay	$t_{d(off)}$	+5V logic			1290			1150	nsec
Shut-down propagation delay (see FIGURE 9)	$t_{Sd}$	$I_O = 30\text{ A peak}$			1100			850	nsec
Turn-on Rise Time	$t_r$	PWR-82340			125			100	nsec
Turn-off Fall Time	$t_f$	$V_{CC} = 140\text{ V}$ PWR-82342 $V_{CC} = 270\text{ V}$			125			150	nsec
<b>DEAD TIME</b>	$t_{dt}$		400			500			nsec
<b>MINIMUM PULSE WIDTH</b>	$t_{pw}$		150			175			nsec
<b>THERMAL</b>									
Maximum Thermal Resistance	$\theta_{j-c}$	each transistor			0.85			0.85	$^\circ\text{C/W}$
Maximum Lead Soldering Temp.	$T_s$	see note 7			250			250	$^\circ\text{C}$
Junction Temperature Range	$T_j$		-55		150	-55		150	$^\circ\text{C}$
Case Operating Temperature	$T_{CO}$		-55		125	-55		125	$^\circ\text{C}$
Case Storage Temperature	$T_{CS}$		-55		150	-55		150	$^\circ\text{C}$
<b>WEIGHT</b>					3.88 (110)			3.88 (110)	oz (g)

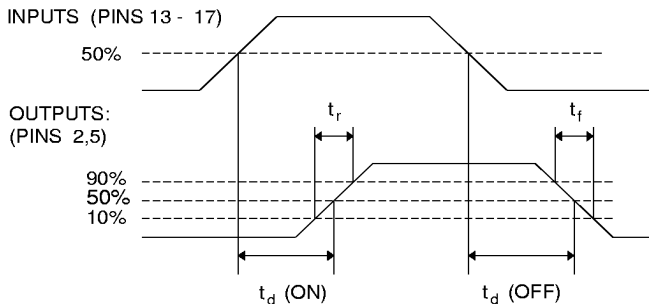
- Notes: 1. For Hi-Rel applications, derating per MIL-S-19500 should be observed. (Derate  $V_{CC}$  to 70%.)  
 2. Pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 3. For PWR-82340  $V_{CC} = 140\text{ V}$ ,  $V_U, V_L = \text{logic '0'}$  and for PWR-82342  $V_{CC} = 350\text{ V}$ ,  $V_U, V_L = \text{logic '0'}$ .  
 4.  $V_U, V_L = \text{logic '0'}$  on pins 13 to 17.  
 5. For PWR-82340  $f_o = 30\text{ kHz}$  and for PWR-82342  $f_o = 10\text{ kHz}$ .  
 6. Pin 12 connected to external +5 V supply.  
 7. Solder 1/8" from case for 5 seconds maximum.

## INTRODUCTION

The PWR-82340 and PWR-82342 are 30 A motor drive hybrids rated at 200 V and 500 V respectively. The PWR-82340 uses a MOSFET output stage and the PWR-82342 has an IGBT output stage for high speed, high current, and high efficiency operation. The PWR-82342 also offers high voltage performance of an IGBT for use in 270 V systems. These motor drives are ideal for use in high performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, Multi-axis systems requiring multiple drive stages can benefit from the small size of these power drives.

The PWR-82340/342 can be driven directly from a PWM, DSP, or a custom ASIC that supplies digital signals to control the

upper and lower transistors of each phase. These highly integrated drive stages have Schmitt trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition by preventing simultaneous turn-on of both the upper and lower transistors. The logic controls the high- and low-side gate drivers. Operation from +5 to +15 V logic levels can be programmed by applying the appropriate voltage to pin 12 ( $V_{LP1}$ ). The PWR-82340/342 has a ground referenced low-side gate drive. An internal DC-DC converter supplies a floating output to each of the two high-side drives. This provides a continuous high-side gate drive even during a motor stall. Pin 11 ( $V_{LPO}$ ) supplies a +15 V output, which can be used to power the internal logic when system usage requires +15 V logic. The high- and low-side gate drivers control the N-channel MOSFET or IGBT output stage. The MOSFETs used in the PWR-82340 allow output switching up to 50 kHz, while the high-speed IGBTs in the PWR-82342 can switch at 25 kHz. A flyback diode parallels each output transistor and controls the regenerative energy produced by the motor. These fast recovery diodes have faster reverse switching times than the intrinsic body diode of the MOSFETs used in the PWR-82340. They also protect the IGBTs used in the PWR-82342 from exceeding their Emitter-to-Collector breakdown voltage. Use of a copper case and solder attachment of the output transistors achieves a low thermal resistance of 0.85  $^\circ\text{C/W}$  maximum. Care should be taken to adequately heatsink these motor drives to maintain a case temperature of +125 $^\circ\text{C}$ . Junction temperatures should not exceed +150 $^\circ\text{C}$ . The PWR-82340/342 does not have internal short circuit or overcurrent protection which, if required, must be added externally to the hybrid.



(Reference TABLE 2 also.)

**FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS**

## BIAS VOLTAGES

The PWR-82340 and PWR-82342 motor drive hybrids only require a single power supply for operation. The hybrid generates two independent, floating supplies, which eliminates the need for external bias voltages for each phase.

In order for the internal power supply to generate these voltages, the input bias voltage ( $V_b$ ) must be from +15 to +50 Vdc. In most avionic systems this can be accomplished by connecting the  $V_b$  pin to the MIL-STD-704D, +28 Volt bus. See FIGURE 3A.

If the system bus voltage is greater than +50 Vdc (and a lower voltage is not available), then the  $V_b$  pin and  $V_z$  pin can be tied

together with an external power resistor ( $R_b$ ) and connected from these pins to the system power bus. See FIGURE 3B.

See FIGURES 4 and 5 for bias resistor characteristics.

If additional power dissipation in  $R_b$  is a concern, FIGURE 3C shows a more efficient design, using a low-power resistor ( $R_0$ ) and an additional transistor. To determine the proper resistor to use, refer to FIGURE 6.

If there is another voltage available in the system in the +15 to +50 VDC range, then this voltage can be directly connected to the  $V_b$  pin of the hybrid. **In any case, a 0.01  $\mu$ f decoupling capacitor ( $C_b$ ) must be connected between  $V_b$  (pin 8) and GND.**

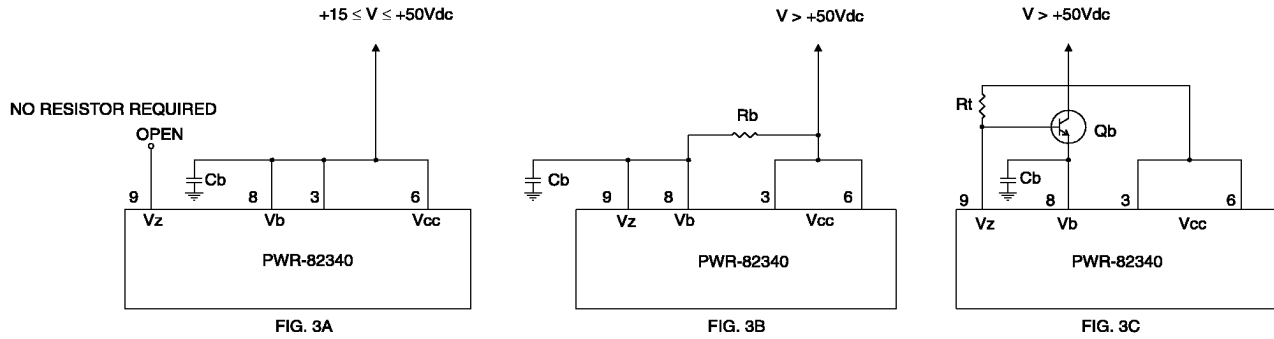


FIGURE 3. CONNECTION TO BUS VOLTAGE TO DEVELOP PROPER INPUT BIAS VOLTAGE

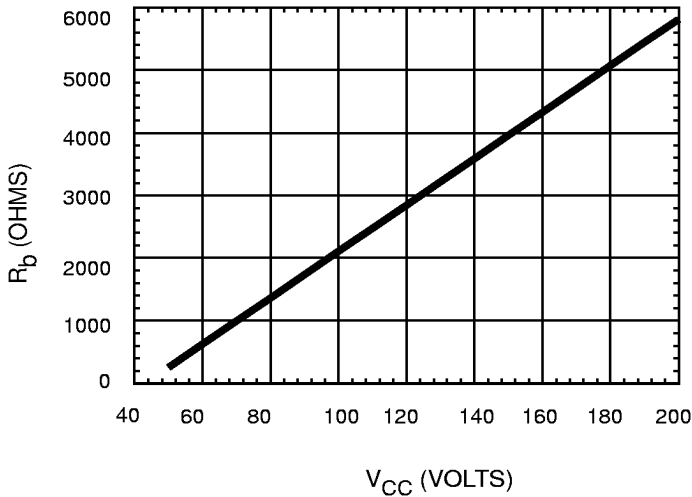


FIGURE 4A. PWR-82340

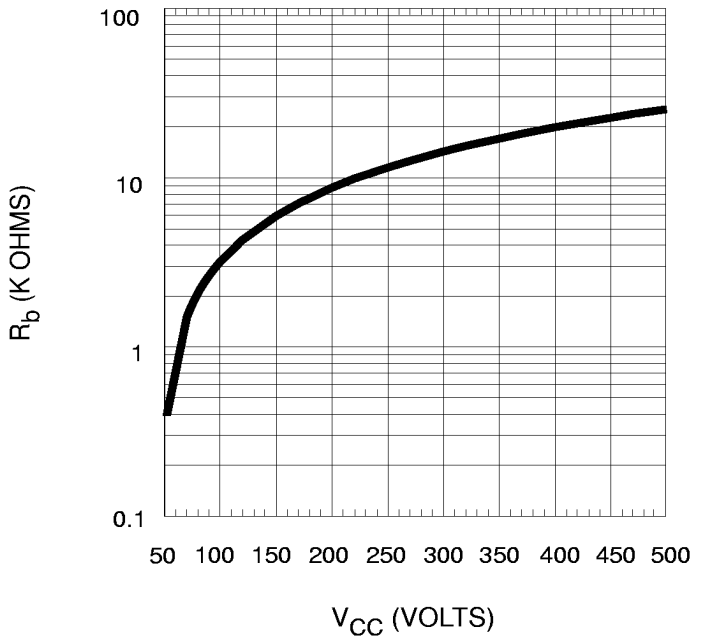


FIGURE 4B. PWR-82342

FIGURE 4. BIAS RESISTOR VALUE VS. BUS VOLTAGE

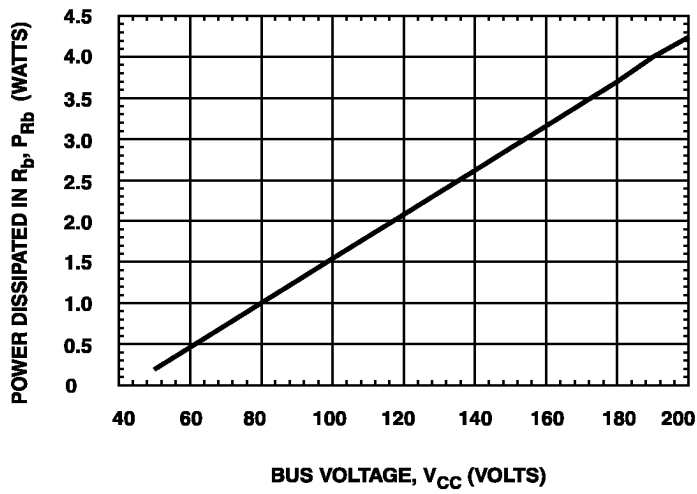


FIGURE 5A. PWR-82340

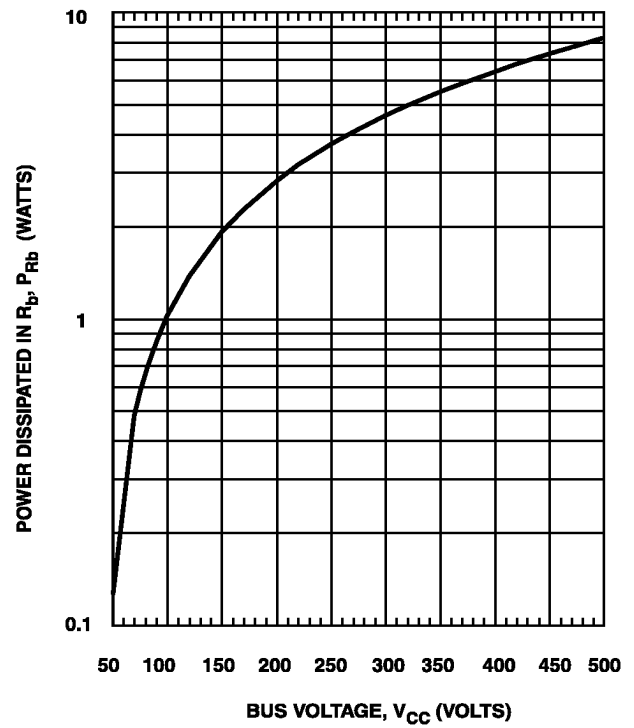


FIGURE 5B. PWR-82342

FIGURE 5. POWER DISSIPATED IN BIAS RESISTOR ( $R_b$ ) VS. BUS VOLTAGE

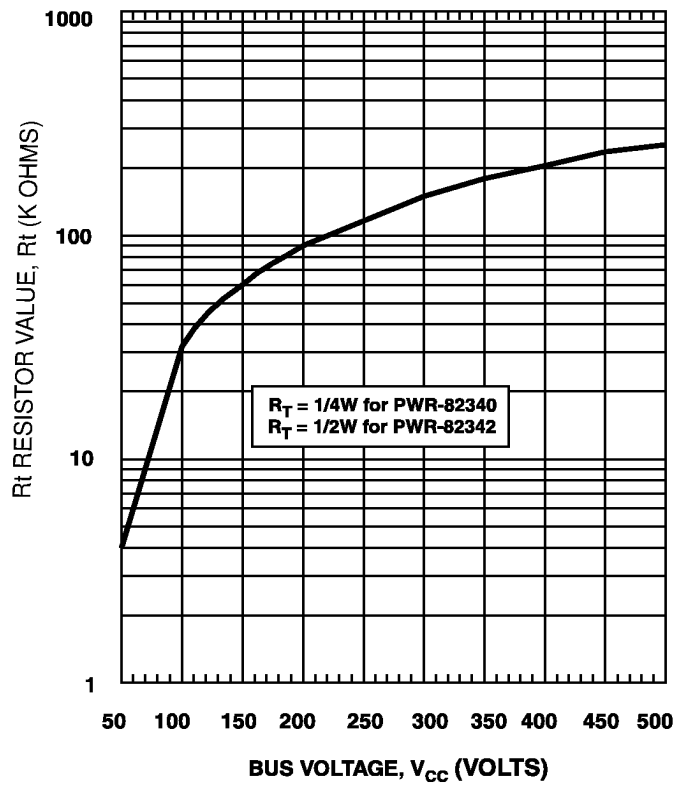


FIGURE 6.  $R_T$  RESISTOR VALUE VS. BUS VOLTAGE

## DIGITALLY CONTROLLED INPUTS

The PWR-82340 and PWR-82342 use Schmitt triggered digital inputs (with hysteresis) to ensure high noise immunity. The trigger switches at different points for positive and negative going signals. Hysteresis voltage ( $V_H$ ) is the difference between the positive going voltage ( $V_P$ ) and the negative going voltage ( $V_N$ ) (see FIGURE 7). The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of control logic with an input voltage range of +5 to +15 V, such as TTL or CMOS logic. The PWR-82340 and PWR-82342 internal power supply generates a +15 Vdc ( $V_{LPO}$ ) on pin 11. This output can only be used to power the internal digital circuitry within the hybrid. **Do not use this +15 V output to power any circuitry**

**external to the hybrid.** Pin 12 is the logic power input ( $V_{LPI}$ ) for the digital circuitry inside the hybrid. **A 0.01  $\mu\text{F}$ , 50 V ceramic capacitor must be placed between this pin (12) and GND as close to the hybrid as possible.** When using 15 V control circuitry, the logic power input (pin 12) can be connected directly to the logic power output (pin 11) of the hybrid. There is no need for an additional external power supply. **When using 5 V control logic, an external +5 VDC supply must be connected between pin 12 of the hybrid, and GND — leave Pin 11 open (N/C).** The control circuitry can be as simple as a PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. The Block Diagram in FIGURE 8 shows a typical interface of the PWR-82340 and PWR-82342 with a motor and control logic in a Servo-Amp System.

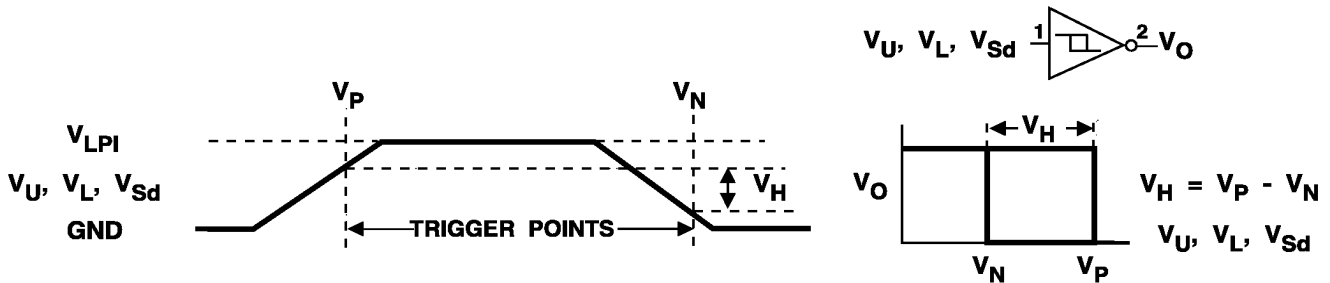


FIGURE 7. HYSTERESIS DEFINITION AND CHARACTERISTICS

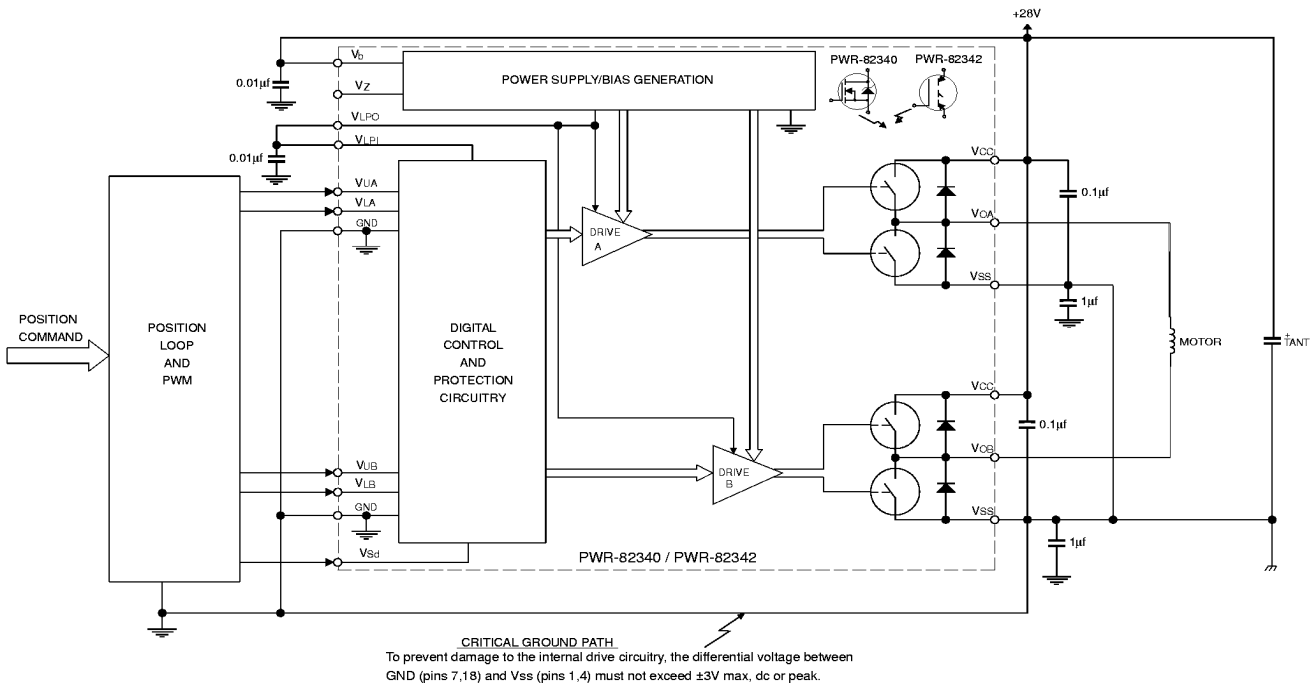


FIGURE 8. PWR-82340/342 TYPICAL INTERFACE WITH A MOTOR AND PWM

## SHUT-DOWN INPUT ( $V_{Sd}$ )

Pin 15 ( $V_{Sd}$ ) provides a digital shut-down input, which allows the user to completely turn off both the upper and lower output transistors in both phases. Application of a logic '1' to the  $V_{Sd}$  input will latch the Digital Control/Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off state and will not respond to signals on the  $V_L$  or  $V_U$  inputs while the  $V_{Sd}$  has a logic '1' applied. When the user or the sense circuitry (as in FIGURE 10) returns the  $V_{Sd}$  input to a logic '0,' and then the user sets the  $V_L$  and  $V_U$  inputs to a logic '0' the output of the Digital Control/Protection circuitry will clear the internal latch. When the next rising edge (see FIGURE 9) occurs on the  $V_L$  or  $V_U$  digital inputs, the output transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs (see FIGURE 10).

## INTERNAL PROTECTION CIRCUITRY

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. FIGURE 9 and TABLE 3 (see page 13) show these timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR- 82340 or PWR-82342. **A dead time of 500 nsec minimum should still be maintained** between the signals at the  $V_U$  and  $V_L$  pins; this ensures the complete turn off of any transistor before turning on its associated in-line transistor.

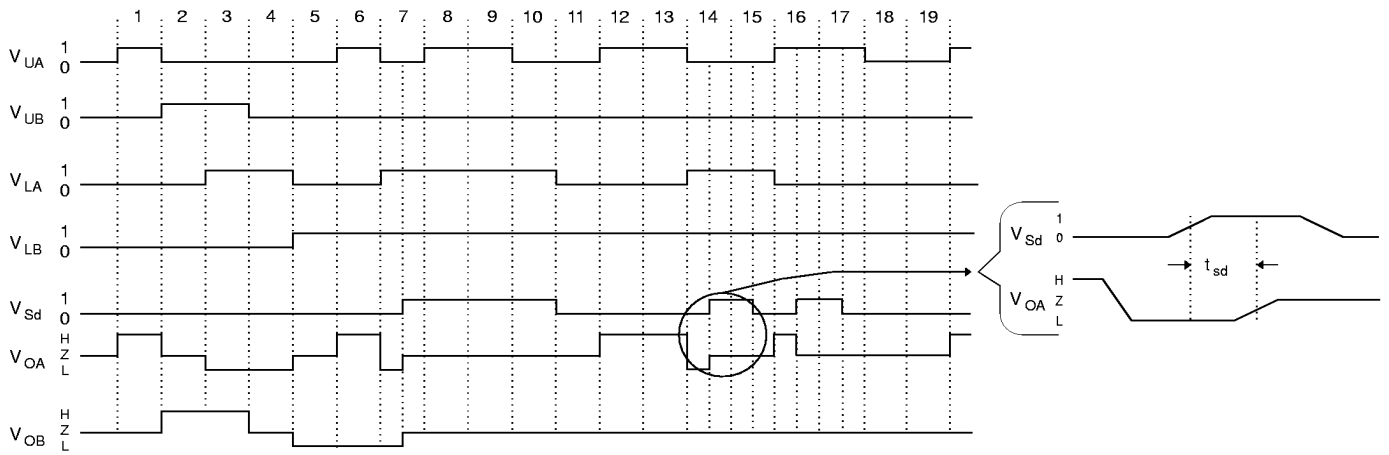


FIGURE 9. SHUT-DOWN ( $V_{Sd}$ ) TIMING RELATIONSHIPS

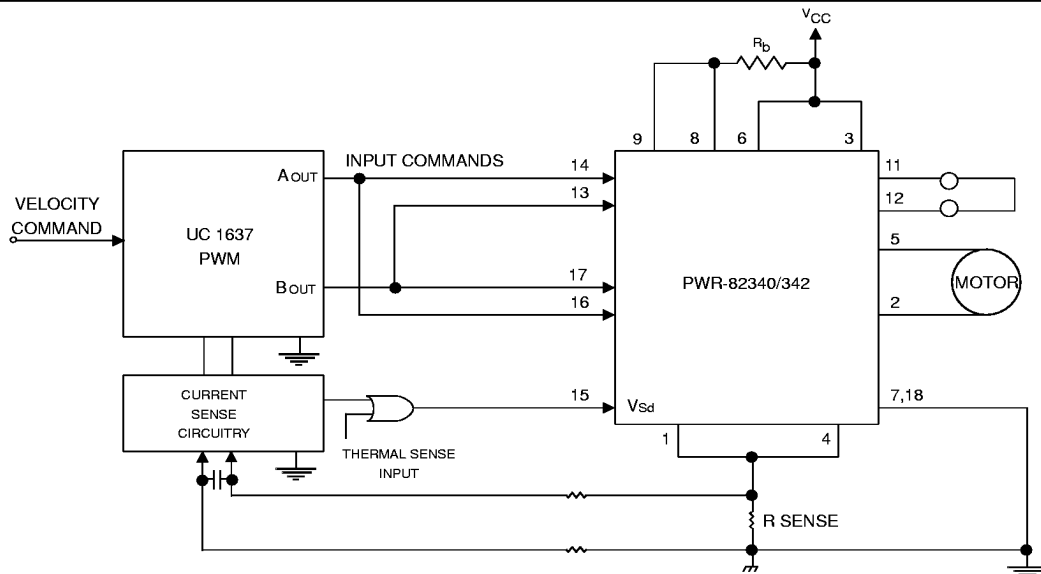


FIGURE 10. FUNCTIONAL SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY

**PWR-82340 POWER DISSIPATION (SEE FIGURE 11)**

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

- $V_{CC} = 140 \text{ V (Bus Voltage)}$
- $I_{OA} = 20 \text{ A (see FIGURE 11)} ; I_{OB} = 30 \text{ A; (see FIGURE 11)}$
- $t_{on} = 20 \mu\text{s (see FIGURE 11)} ; T = 40 \mu\text{s (period)}$
- $R_{on} = 0.1 \Omega$  (on resistance see TABLE 2,  $I_o = 30 \text{ A}, T_c = 25 \text{ }^\circ\text{C}$ )
- $t_{s1} = 250 \text{ ns (see FIGURE 11)} ; t_{s2} = 250 \text{ ns (see FIGURE 11)}$
- $f_o = 25 \text{ kHz (switching frequency)}$
- $V_f$  is the diode forward voltage, Table 2,  $I_o = 30 \text{ A}, T_c = 25 \text{ }^\circ\text{C}$
- $V_{f(avg)} = 1.15 \text{ V}$
- $I_f$  is the diode forward current

**1. Conduction Losses ( $P_C$ )**

$$P_C = I(t)^2 \times R_{on} = I_{\text{motor rms}}^2 \times R_{on}$$

$$I_{\text{motor rms}} = \sqrt{\left( I_{OB}^2 - I_{OB}(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3} \right) \left( \frac{t_{on}}{T} \right)}$$

$$I_{\text{motor rms}} = \sqrt{\left( 30^2 - 30(30 - 20) + \frac{(30 - 20)^2}{3} \right) \left( \frac{20}{40} \right)}$$

$$P_C = (17.80 \text{ A})^2 \times (0.1 \Omega)$$

$$P_C = 31.68 \text{ Watts}$$

**2. Switching Losses ( $P_S$ )**

$$P_S = \{V_{CC} [I_{OA}(t_{s1}) + I_{OB}(t_{s2})] f_o\} / 2$$

$$P_S = \{140 [20(250 \text{ ns}) + 30(250 \text{ ns})] 25k\} / 2$$

$$P_S = 21.88 \text{ Watts}$$

**3. Flyback diode Losses ( $P_{df}$ )**

$$P_{df} = I_f(\text{avg}) \times V_f(\text{avg})$$

$$I_f(\text{avg}) = [(I_{OB} + I_{OA}) / 2] / 2 = [(30 + 20) / 2] / 2 = 12.5 \text{ A}$$

$$P_{df} = 12.5 \text{ A} \times 1.15 \text{ V}$$

$$P_{df} = 14.38 \text{ Watts}$$

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

To calculate Total Power dissipated in the hybrid use:

$$P_{\text{Total}} = \sum_{i=1}^4 [P_{ci} + P_{si} + P_{dfi}] \text{ where } i = \text{each transistor or diode.}$$

**PWR-82342 POWER DISSIPATION (SEE FIGURE 11)**

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

- $V_{CC} = 270 \text{ V (Bus Voltage)}$
- $I_{OA} = 20 \text{ A (see FIGURE 11)} ; I_{OB} = 30 \text{ A; (see FIGURE 11)}$
- $t_{on} = 50 \mu\text{s (see FIGURE 11)} ; T = 100 \mu\text{s (period)}$
- $V_{CE(SAT)} = 3.8 \text{ V (see TABLE 2, } I_o = 30 \text{ A, } T_c = 25 \text{ }^\circ\text{C)}$
- $t_{s1} = 300 \text{ ns (see FIGURE 11)} ; t_{s2} = 300 \text{ ns (see FIGURE 11)}$
- $f_o = 10 \text{ kHz (switching frequency)}$
- $V_f$  is the diode forward voltage, TABLE 2,  $I_o = 30 \text{ A}, T_c = 25 \text{ }^\circ\text{C}$
- $V_{f(avg)} = 1.70 \text{ V}$
- $I_f$  is the diode forward current

**1. Conduction Losses ( $P_C$ )**

$$P_C = I(t)^2 \times V_{CE(SAT)} = I_{AVG} \times V_{CE(SAT)}$$

$$I_{AVG} = \left( \frac{(I_{OB} + I_{OA})}{2} \right) \left( \frac{t_{on}}{T} \right)$$

$$I_{AVG} = \left( \frac{(30 + 20)}{2} \right) \left( \frac{50}{100} \right)$$

$$P_C = (12.5 \text{ A}) \times (3.8 \text{ V})$$

$$P_C = 47.50 \text{ Watts}$$

**2. Switching Losses ( $P_S$ )**

$$P_S = \{V_{CC} [I_{OA}(t_{s1}) + I_{OB}(t_{s2})] f_o\} / 2$$

$$P_S = \{270 [20(300 \text{ ns}) + 30(300 \text{ ns})] 10k\} / 2$$

$$P_S = 20.25 \text{ Watts}$$

**3. Flyback diode Losses ( $P_{df}$ )**

$$P_{df} = I_s(\text{avg}) \times V_f(\text{avg})$$

$$I_f(\text{avg}) = [(I_{OB} + I_{OA}) / 2] / 2 = [(30 + 20) / 2] / 2 = 12.5 \text{ A}$$

$$P_{df} = 12.5 \text{ A} \times 1.70 \text{ V}$$

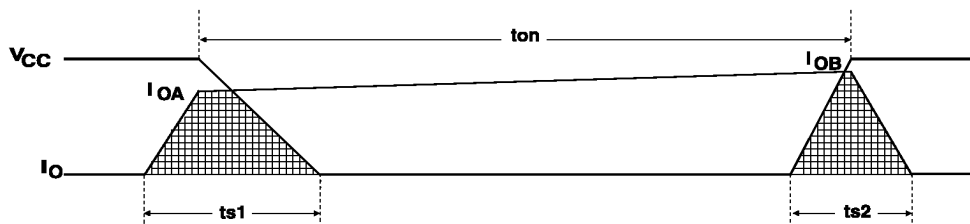
$$P_{df} = 21.25 \text{ Watts}$$

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

To calculate Total Power dissipated in the hybrid use:

$$P_{\text{Total}} = \sum_{i=1}^4 [P_{ci} + P_{si} + P_{dfi}] \text{ where } i = \text{each transistor or diode.}$$



**FIGURE 11. OUTPUT CHARACTERISTICS**



## GROUND CONNECTIONS

### LAYOUT AND EXTERNAL COMPONENTS

**Important Information** - The following information regarding layout guidelines and required external components is critical to the proper operation of these motor drives.

External connections can be easily made to the hybrid by any of the following methods:

- Solder a wire around each pin.
- Use a printed circuit board with a cutout that will enable the printed circuit board to slide over the pins.

**Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.**

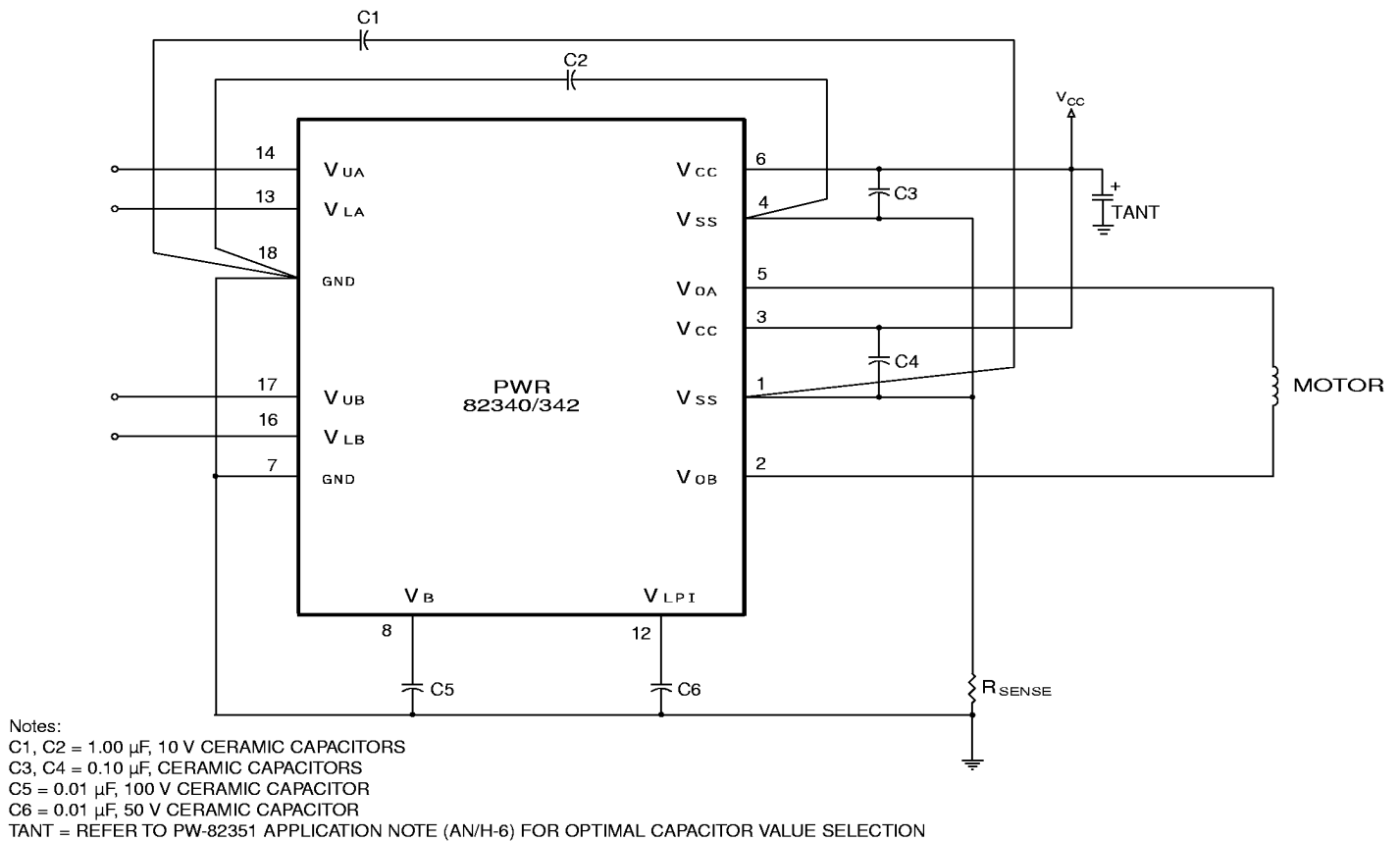
The  $V_b$  and logic grounds are on pins 7 and 18 (GND). The  $V_{ss}$  connections for the output stage are on pins 1 and 4 ( $V_{ss}$ ). **To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 7, 18) and  $V_{ss}$  (pins 1, 4) must not exceed  $\pm 3$  V max, dc or peak.** This includes the combined voltage drop of the associated ground paths and the voltage drop across  $R_{sense}$  (see FIGURE 12). For example, a value for  $R_{sense}$  of  $0.025 \Omega$  will give a voltage drop of 1.25 V at 50 A and

allow enough margin for the voltage drop in the ground conductors. Locate  $R_{sense}$  1" - 2" maximum from the hybrid. **It is critical that all ground connections be as short, and of lowest impedance, as the system allows.**

C1 and C2 are 1  $\mu$ F, 10 V ceramic capacitors that provide a low ac impedance between each  $V_{ss}$  pin and GND. You must use one capacitor for each  $V_{ss}$  pin-to-GND connection (total of two capacitors in all). These capacitors are independent of the type of drive scheme used. Since placement of these capacitors is critical, place these capacitors across the hybrid, if possible. Please note, on FIGURE 12, that C1 and C2 must go directly from terminal to terminal on the hybrid — **do not daisy chain along the ground return.**

C3 and C4 are the 0.1  $\mu$ f ceramic bypass capacitors that suppress high frequency spiking. The voltage rating should be 2x the maximum system voltage. These capacitors should be located as close to the hybrid as possible.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the  $V_{cc}$  line. Accomplish this by placing a capacitor or clamping diode between  $V_{cc}$  and the high power ground return.



**FIGURE 12. PWR-82340/342 GROUND CONNECTIONS**

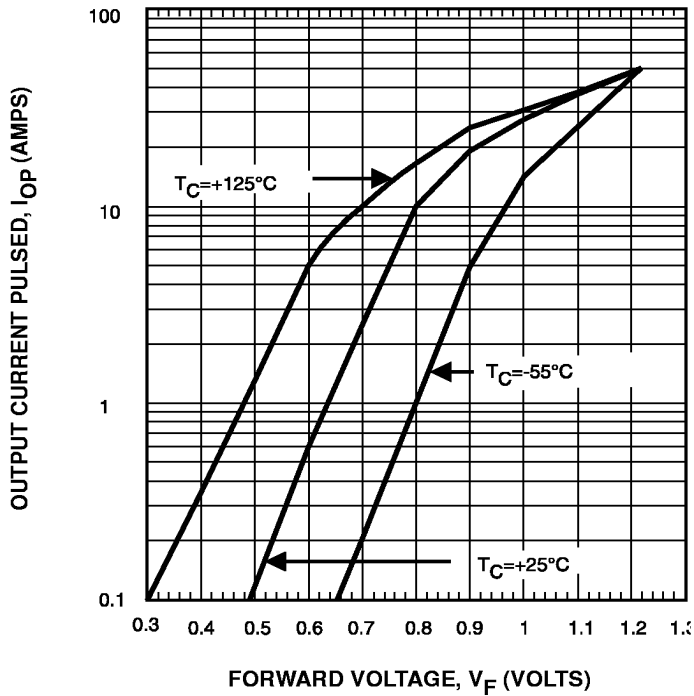


FIGURE 13A. PWR-82340 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES

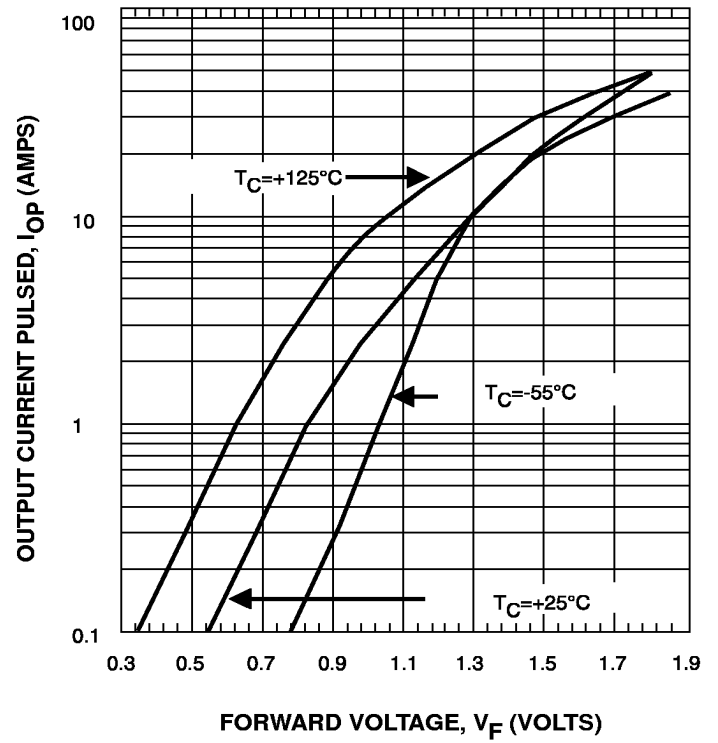


FIGURE 13B. PWR-82342 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES

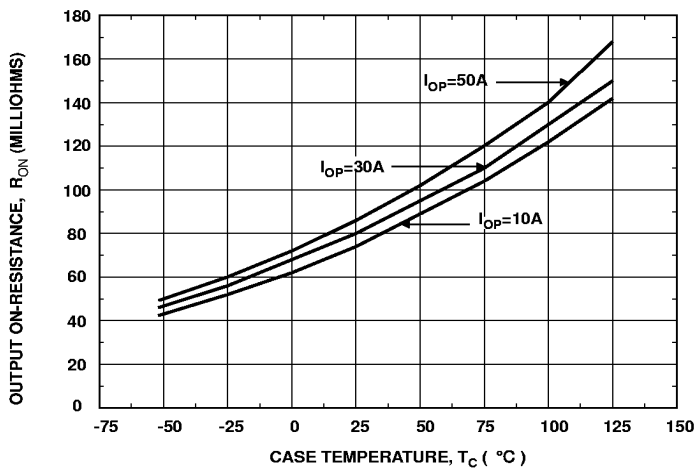


FIGURE 14A. PWR-82340 TYPICAL ON RESISTANCE VARIATION WITH TEMPERATURE

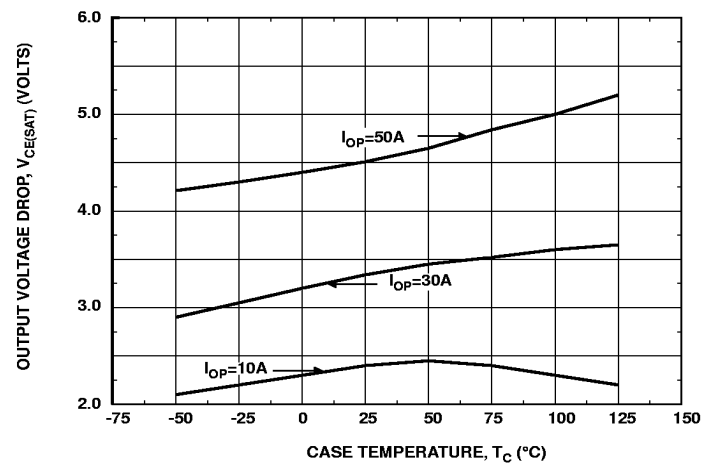


FIGURE 14B. PWR-82342 TYPICAL VCE(SAT) VARIATION WITH TEMPERATURE

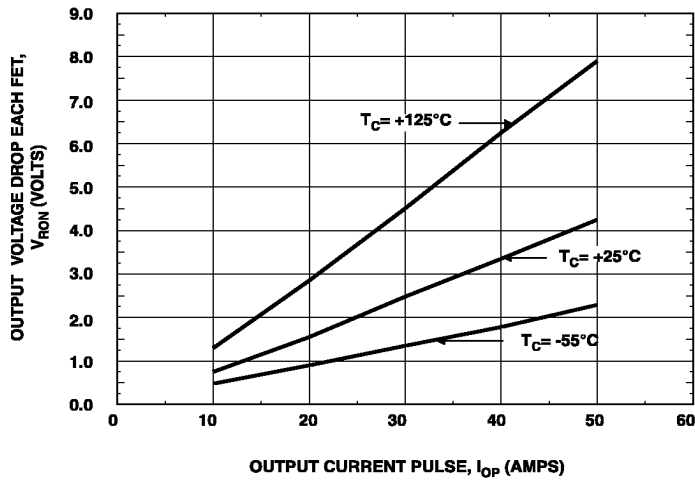


FIGURE 15A. PWR-82340 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT

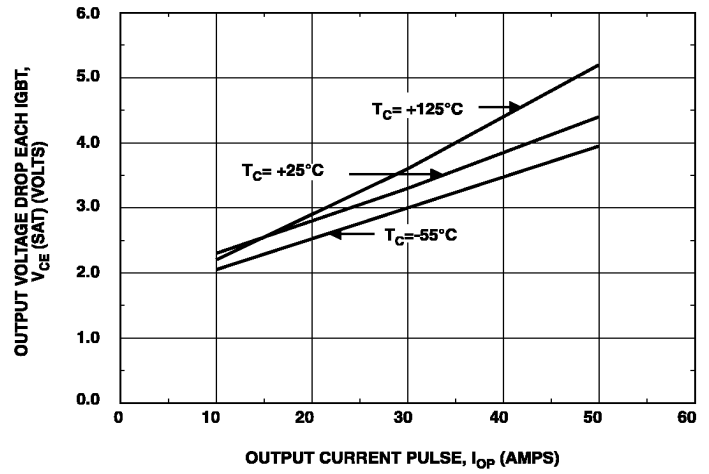


FIGURE 15B. PWR-82342 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT

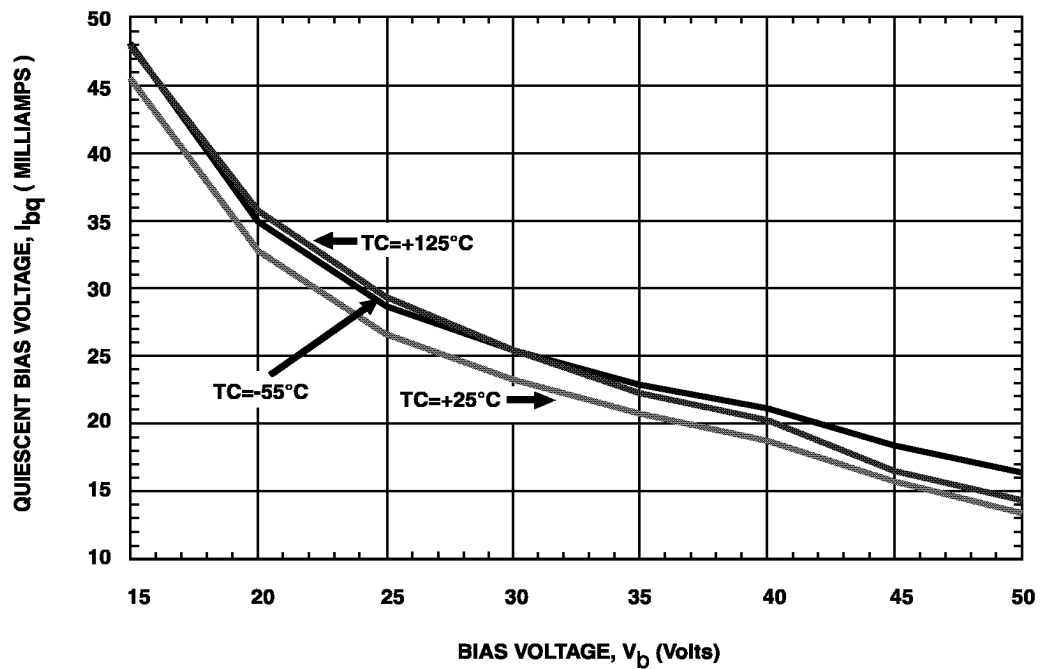


FIGURE 16. PWR-82340/342 TYPICAL QUIESCENT BIAS CURRENT VERSUS BIAS VOLTAGE

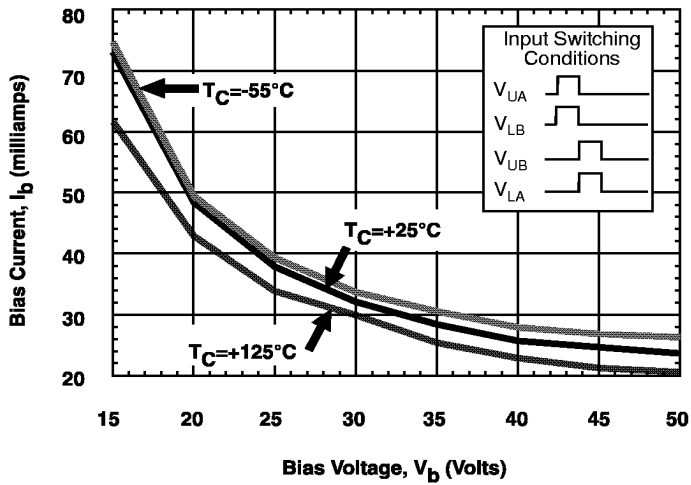


FIGURE 17A. PWR-82340 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE AT  $F_0 = 30$  KHZ

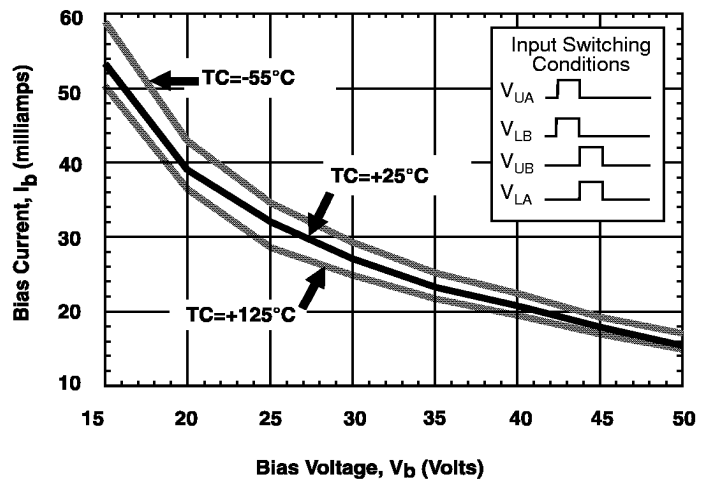


FIGURE 17B. PWR-82342 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE AT  $F_0 = 10$  KHZ

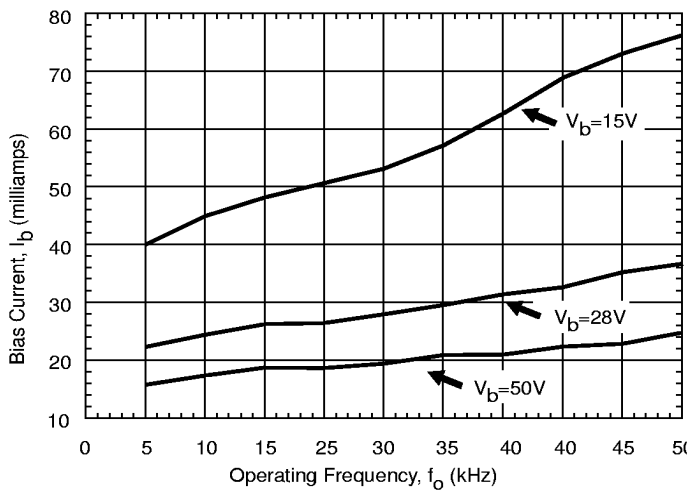


FIGURE 18A. PWR-82340 BIAS CURRENT VERSUS OPERATING FREQUENCY

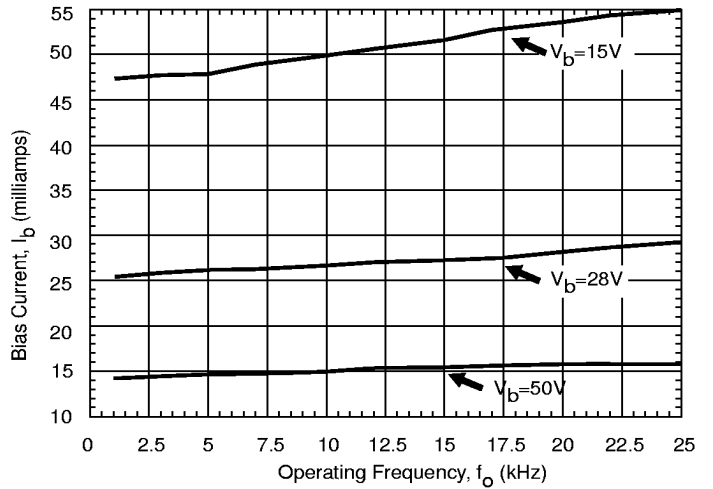
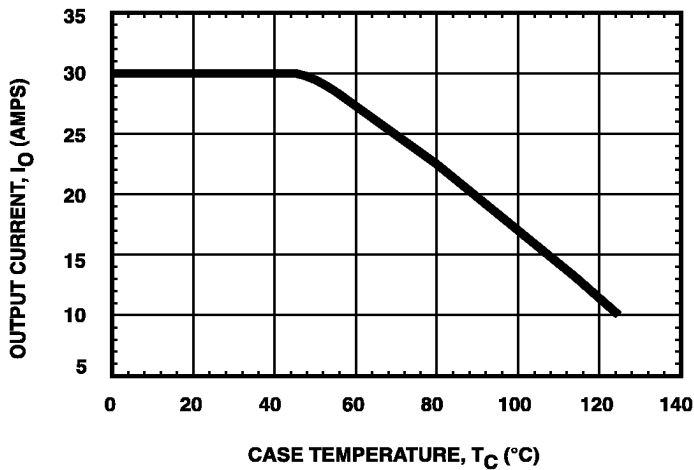


FIGURE 18B. PWR-82342 BIAS CURRENT VERSUS OPERATING FREQUENCY

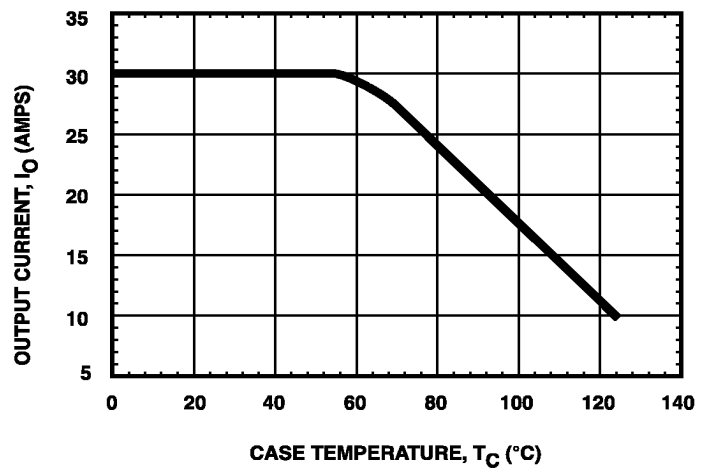
## MOUNTING

The package bolts to part of the chassis or even the motor assembly itself, depending on system requirements. In applications where this isn't convenient, the hybrid can be mounted to its own heatsink. The heat transfer in a hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and

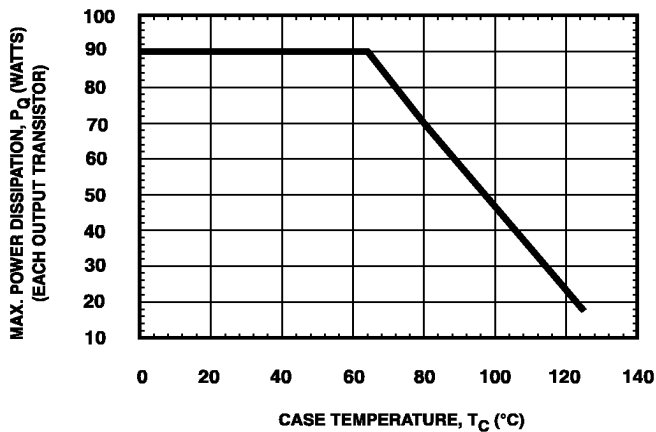
maximum temperature of this mounting surface are critical to proper performance and reliability, because this is the only method of dissipating the power created in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad. The heatsink should be designed to insure that the case temperature does not exceed +125°C



**FIGURE 19A. PWR-82340  
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT  
CURRENT VERSUS CASE TEMPERATURE**



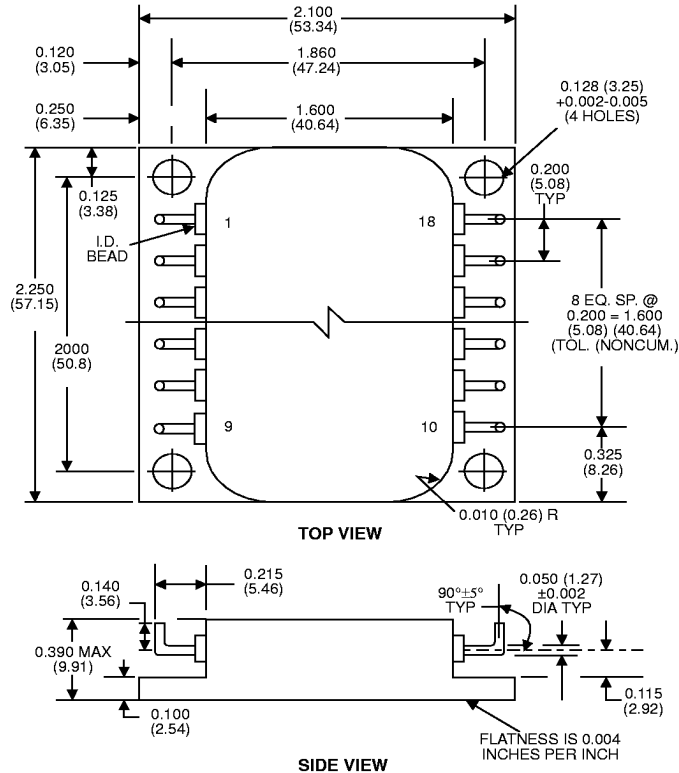
**FIGURE 19B. PWR-82342  
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT  
CURRENT VERSUS CASE TEMPERATURE**



**FIGURE 20. PWR-82340 AND PWR-82342 MAXIMUM  
ALLOWABLE POWER DISSIPATION  
OF EACH OUTPUT TRANSISTOR VERSUS CASE  
TEMPERATURE**

TABLE 3. INPUT-OUTPUT TRUTH TABLE						
INPUTS						OUTPUTS
UPPERS		LOWERS		CONTROL		
$V_{UA}$	$V_{UB}$	$V_{LA}$	$V_{LB}$	$V_{Sd}$	$V_{OA}$	$V_{OB}$
0	0	1	1	0	L	L
0	1	1	0	0	L	H
1	0	0	1	0	H	L
1	1	0	0	0	H	H
1	X	1	X	0	Z	X
X	1	X	1	0	X	Z
0	0	0	0	0	Z	Z
X	X	X	X	1	Z	Z

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off)



NOTE: Dimensions in inches (mm).

**FIGURE 21. PWR-82340 AND PWR-82342 MECHANICAL OUTLINE**

TABLE 4. PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	V <sub>SS</sub>	18	GND
2	V <sub>OB</sub>	17	V <sub>UB</sub>
3	V <sub>CC</sub>	16	V <sub>LB</sub>
4	V <sub>SS</sub>	15	V <sub>Sd</sub>
5	V <sub>OA</sub>	14	V <sub>UA</sub>
6	V <sub>CC</sub>	13	V <sub>LA</sub>
7	GND	12	V <sub>LPI</sub>
8	V <sub>b</sub>	11	V <sub>LPO</sub>
9	V <sub>Z</sub>	10	N/C

Note: Pins 3 and 6 are internally connected;  
Pins 7 and 18 are internally connected.

# NOTES

## ORDERING INFORMATION

PWR-8234X -X X 0

**Reliability Grade:**

- 0 = Standard DDC Procedures.
- 1 = Military processing available.
- 2 = Military processing available without QCI testing.

**Temperature Range:**

- 1 = -55 to +125°C
- 3 = 0 to +70°C

**Rating:**

- 0 = 200 V using MOSFETs
- 2 = 500 V using IGBTs

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The information provided in this data sheet is believed to be accurate; however, no responsibility is assumed by ILC Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.



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